AMENDMENTS TO THE CLAIMS

1. (Original) A memory system, comprising:

a memory cell;

first and second bitlines operably connected to said memory cell;

a write line operably connected to said memory cell; and

an equilibration circuit connected to said first and second bitlines, wherein said equilibration circuit is operable to maintain a predetermined equilibrium condition between said first and second bit lines and wherein said equilibration circuit is controlled by a reference voltage.

2. (Original) The memory system according to claim 1, wherein said equilibration circuit is operable to generate an impedance load in said first and second bit lines at a level that allows generation of differential signals in said bit lines.

3. (Original) The memory system according to claim 2, wherein said equilibration circuit comprises first and second pMOS devices in series with said first and second bitlines, respectively, and a third pMOS device connected between said first and second bitlines and wherein the gates of said first, second and third pMOS devices are connected to said reference voltage.

4. (Currently Amended) A memory system, comprising:

a memory cell;

first and second bitlines operably connected to said memory cell;

a write line operably connected to said memory cell; and

an equilibration circuit controlled by a reference voltage, said equilibrium circuit connected to said first and second bitlines, said equilibrium circuit comprising first and second pMOS devices in series with said first and second bitlines, respectively, and a third pMOS device connected between said first and second bitlines and wherein the gates of said first, second and third pMOS devices are connected to said reference voltage, ~~The memory system according to claim 3~~, wherein said first, second and third

pMOS devices operate as resistors in the linear region of MOSFET device operation, and wherein said equilibration circuit is operable:

to maintain a predetermined equilibrium condition between said first and second bit lines; and

to generate an impedance load in said first and second bit lines at a level that allows generation of differential signals in said bit lines.

5. (Original) The memory system according to claim 4, wherein the resistance of said first, second and third pMOS devices is determined by the gate-source voltage of said pMOS devices.

6. (Original) The memory system according to claim 5, wherein said write line is operably connected to said memory cell by at least one transfer gate.

7. (Original) The memory system according to claim 6, wherein said transfer gate comprises an nMOS device and wherein said reference voltage is related to the gate drive current of said transfer gate.

8. (Original) The memory system according to claim 7, wherein said reference voltage is controlled by a reference circuit that is operable to change said reference voltage to compensate for variations in operating characteristics of said first, second and third pMOS devices.

9. (Original) The memory system according to claim 8, wherein said reference circuit is further operable to change the reference voltage to compensate for variations in the operating characteristics of said nMOS device comprising said transfer gate.

10. (Original) The memory system according to claim 9, wherein said reference circuit comprises a current mirror.

11. (Original) A method for controlling operation of a memory system, comprising:

storing information in a memory cell;

generating a predetermined equilibrium condition between first and second bitlines operably connected to said memory cell using an equilibration circuit connected to said first and second bitlines, wherein said equilibration circuit is controlled by a reference voltage; and

controlling the content of information in said memory cell with a write line operably connected to said memory cell.

12. (Original) The method according to claim 11, wherein said equilibration circuit is operable to generate an impedance load in said first and second bit lines at a level that allows generation of differential signals in said bit lines.

13. (Original) The method according to claim 12, wherein said equilibration circuit comprises first and second pMOS devices in series with said first and second bitlines, respectively, and a third pMOS device connected between said first and second bitlines and wherein the gates of said first, second and third pMOS devices are connected to said reference voltage.

14. (Currently Amended) A method for controlling operation of a memory system, comprising:

storing information in a memory cell;

generating a predetermined equilibrium condition between first and second bitlines operably connected to said memory cell using an equilibration circuit connected to said first and second bitlines, said equilibrium circuit being controlled by a reference voltage and comprising first and second pMOS devices in series with said first and second bitlines, respectively, and a third pMOS device connected between said first and second bitlines, wherein the gates of said first, second and third pMOS devices are connected to said reference voltage and, ~~The method according to claim~~

~~13~~, wherein said first, second and third pMOS devices operate as resistors in the linear region of MOSFET device operation; and

controlling the content of information in said memory cell with a write line operably connected to said memory cell.

15. (Original) The method according to claim 14, wherein the resistance of said first, second and third pMOS devices is determined by the gate-source voltage of said pMOS devices.

16. (Original) The method according to claim 15, wherein said write line is operably connected to said memory cell by at least one transfer gate.

17. (Original) The method according to claim 16, wherein said transfer gate comprises an nMOS device and wherein said reference voltage is related to the gate drive current of said transfer gate.

18. (Original) The method according to claim 17, wherein said reference voltage is controlled by a reference circuit that is operable to change said reference voltage to compensate for variations in operating characteristics of said first, second and third pMOS devices.

19. (Original) The method according to claim 18, wherein said reference circuit is further operable to change the reference voltage to compensate for variations in the operating characteristics of said nMOS device comprising said transfer gate.

20. (Original) The method according to claim 19, wherein said reference circuit comprises a current mirror.

21. (Original) A digital processing system, comprising:

a datapath module;

a control module;

an input-output module; and

a memory module, wherein said memory module comprises:

at least one memory cell;

first and second bitlines operably connected to said memory cell;
a write line operably connected to said memory cell; and
an equilibration circuit connected to said first and second bitlines, wherein said equilibration circuit is operable to maintain a predetermined equilibrium condition between said first and second bit lines and wherein said equilibration circuit is controlled by a reference voltage.

22. (Currently Amended) The ~~method~~ digital processing system according to claim 21, wherein said equilibration circuit is operable to generate an impedance load in said first and second bitlines at a level that allows generation of differential signals in said bitlines.

23. (Currently Amended) The ~~method~~ digital processing system according to claim 22, wherein said equilibration circuit comprises first and second pMOS devices in series with said first and second bitlines, respectively, and a third pMOS device connected between said first and second bitlines and wherein the gates of said first, second and third pMOS devices are connected to said reference voltage.

24. (Currently Amended) A digital processing system, comprising:
a datapath module;
a control module;
an input-output module; and
a memory cell;
first and second bitlines operably connected to said memory cell;
a write line operably connected to said memory cell; and
an equilibration circuit controlled by a reference voltage, said equilibrium circuit connected to said first and second bitlines, said equilibrium circuit comprising first and second pMOS devices in series with said first and second bitlines, respectively, and a third pMOS device connected between said first and second bitlines and wherein the gates of said first, second and third pMOS devices are connected to said reference voltage, ~~The~~

~~method according to claim 23~~, wherein said first, second and third pMOS devices operate as resistors in the linear region of MOSFET device operation, wherein said equilibration circuit is operable:

to maintain a predetermined equilibrium condition between said first and second bit lines; and

to generate an impedance load in said first and second bit lines at a level that allows generation of differential signals in said bit lines.

25. (Currently Amended) The ~~method~~ digital processing system according to claim 24, wherein the resistance of said first, second and third pMOS devices is determined by the gate-source voltage of said pMOS devices.

26. (Currently Amended) The ~~method~~ digital processing system according to claim 25, wherein said write line is operably connected to said memory cell by at least one transfer gate.

27. (Currently Amended) The ~~method~~ digital processing system according to claim 26, wherein said transfer gate comprises an nMOS device and wherein said reference voltage is related to the gate drive current of said transfer gate.

28. (Currently Amended) The ~~method~~ digital processing system according to claim 27, wherein said reference voltage is controlled by a reference circuit that is operable to change said reference voltage to compensate for variations in operating characteristics of said first, second and third pMOS devices.

29. (Currently Amended) The ~~method~~ digital processing system according to claim 28, wherein said reference circuit is further operable to change the reference voltage to compensate for variations in the operating characteristics of said nMOS device comprising said transfer gate.

30. (Currently Amended) The ~~method~~ digital processing system according to claim 29, wherein said reference circuit comprises a current mirror.